CS 315

Assignment 2 – part 3
Gate Design

1) The following problems from the attached page:

2-32
2-33
2-39 (figure 2-36 below)

Fig. 2-36 Implementing \( F = (AB + AB) \cdot (C + D) \) with NOR Gates
2-32. Convert the AND/OR/NOT logic diagram in Figure 2-46 to a) a NAND logic diagram and b) a NOR logic diagram.

2-33. The following function is to be implemented with a minimum gate multilevel circuit (three or more levels of gates not counting inverters on the inputs or output). Assume the complements of the inputs are not available.

\[ F(A, B, C, D) = \overline{ABCD} + \overline{ABC}D + ABCD + AB\overline{CD} \]

(a) Use NAND gates only.
(b) Use NOR gates only.

2-34. *Prove that the dual of the exclusive-OR is also its complement.

2-35. Derive the exclusive-OR/exclusive-NOR circuits for a three-bit parity generator and a four-bit parity checker, using an even parity bit.

2-36. Implement the Boolean function in problem 2-28(b) with exclusive-OR and AND gates.

2-37. *An integrated circuit logic family has NAND gates with a fan-out of 8 standard loads and buffers with a fan-out of 16 standard loads. Show how the output signal of a single NAND gate can be applied to 38 other gate inputs using buffers. Assume that each input is one standard load.

2-38. +A NAND gate with eight inputs is required. For each of the following cases, minimize the number of gates used in the multiple-level result:
(a) Design the 8-input NAND gate using 2-input NAND gates and NOT gates.
(b) Design the 8-input NAND gate using 2-input NAND gates, 2-input NOR gates, and use NOT gates only if needed.
(c) Compare the number of gates used in (a) and (b).

2-39. *The NOR (and NOT) gates in Figure 2-36 have propagation delay \( t_{pd} = 0.5 \) ns. What is the propagation delay of the longest path through the circuit?