Memory Systems

Chapter 10
Memory Systems
Introduction

- A number of different types of memories and programmable logic devices exist.
  - Random-access memory (RAM)
  - Read-only memory (ROM)
  - Programmable logic devices (PLDs)
    - Programmable logic arrays (PLAs)
    - Programmable array logic (PAL)
    - Programmable gate arrays (PGAs)
  - Programmable sequential arrays (PSAs)
  - Field-programmable gate arrays (FPGAs)
- Due to time limitations, we will only cover RAM.
Memory Systems
Types of RAM

- Two main categories of random-access memory (RAM) exist.
  - Static memory or static RAM (SRAM)
    - Information bits are latched such as with a latch or a flip-flop.
    - Typical SRAM implementations require 4 to 6 transistors.
  - Dynamic memory or dynamic RAM (DRAM)
    - Information bits are stored in the form of electric charges on capacitors.
    - The capacitors will discharge over time.
    - Refreshing the memory cell is required before the capacitor has discharged to much of the electric charge.
    - Most DRAM implementations use 1 transistor and 1 capacitor.
Static RAM
SRAM CELLS

- An inefficient SRAM bit cell can be formed as follows.
  Select (word line)

- How many transistors required for this design?
  - 2*4 for inverters + 2*2 for TGs = 12 transistors.
  - Very expensive in terms of silicon real estate!!!
Dynamic RAM
DRAM Cells

- A dynamic RAM cell stores the bit as a charge in a capacitor.
- This bit must be refreshed periodically (>100s of times a second).

Select (word line)

Transmission gate opens when selected to charge or discharge capacitor.
This charge stores the bit.

- How many transistors required for this design?
  - 2*1 for TG and 2*1 for inverter = 4 transistors.
  - Still expensive considering the extra refresh circuitry required!
Memory Units
Specification

- Having developed bit cells, either SRAM or DRAM bit cells, they can now be pieced together forming a memory unit.

- What do we want to specify in the design of a memory unit?
  - The number of bits.
    - This gives the total number of bits that the memory unit can store.
  - The grouping of bits into words.
    - Accessing 1 bit at a time might be inconvenient, so, grouping bits into words is often done.
    - Common examples of word bit sizes are 4, 8, 16, 32, and 64.
  - The number of words in the memory unit (addressable words).
    - This is a function of the word size and total number of bits.
Memory Units
Description

- In describing the capacity of a memory unit, the following is used
  - \# addresses x word size
    - Example: 1Mx8

- If a memory unit is described as 1Mx8, then it has
  - \(1\text{M} = 2^{20} = 1048576\) addresses,
  - 8 bits per word at each address location,
  - 8 data lines for the 8 bit words,
  - 20 address lines to specify the \(1\text{M} = 2^{20} = 1048576\) addresses,
  - and \((1048576)(8) = 8388608\) bits in the entire memory unit.
Memory Units
Description Examples

- Some further examples of memory descriptions are given below.
- Note that the last four columns are all described with the information in the first column.
- Try to fill in the empty cells for the last two rows.

<table>
<thead>
<tr>
<th>Memory</th>
<th>Total bits</th>
<th># of addresses</th>
<th># address lines</th>
<th># data lines</th>
</tr>
</thead>
<tbody>
<tr>
<td>1Mx8</td>
<td>8388608</td>
<td>1048576</td>
<td>20</td>
<td>8</td>
</tr>
<tr>
<td>1Kx4</td>
<td>4096</td>
<td>1024</td>
<td>10</td>
<td>4</td>
</tr>
<tr>
<td>2Mx4</td>
<td>8388608</td>
<td>2097152</td>
<td>21</td>
<td>4</td>
</tr>
<tr>
<td>4Mx1</td>
<td>4194304</td>
<td>4194304</td>
<td>22</td>
<td>1</td>
</tr>
<tr>
<td>2Mx32</td>
<td>67108864</td>
<td>2097152</td>
<td>21</td>
<td>32</td>
</tr>
<tr>
<td>16Kx64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8Mx8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Memory Units
Block Diagram (1)

- Below is a general block diagram for a memory unit.

- The $k$ address lines access a word in the memory for input or output.
- To simplify drawing, we now form busses of $n$ (or $k$) lines.
Memory Units
Block Diagram (2)

- To conserve pins, the following layout is more common in practice.

- The data lines are both input and output lines (not simultaneously).
  - This is done by using tristate buffers to form a tristate bus (or sometimes referred to as a three-state bus).
Memory Units
Internal Structure

- The bit cells are arranged in matrix. (more efficient!)
- Row and column decoders access specific bit cells.
Memory Units
Read/Write of 1-bit

- In read mode:
  - Row decoder “activates” all bit cells in that row.
    - Each bit cell in the row outputs their stored bit.
  - Column decoder takes the bit from only one column of the activated row.
- In write mode:
  - Row decoder “activates” all bit cells in that row.
    - Each bit cell in the row effectively outputs their stored bit.
  - Column decoder selects the appropriate column and writes the input bit.
    - SRAM: This writing is done by “overpowering” what is being read by the bit cell with a stronger voltage/current.
    - DRAM: This writing is done by recharging the capacitor for writing a 1 or discharging the capacitor for writing a 0.
Memory Units
Control Lines (1)

- Now include \( k \) address lines, 1-bit data line, Enable, and \(~\)Read/Write.
Memory Units
Control Lines (2)

• Things to note about the previous implementation.
  • The *k address lines* are split into two parts (not necessarily equal parts)
    • *p* of the *k* address lines are sent to the *row decoder*.
    • *k-p* of the *k* address lines are sent to the column decoder.
  • There is only one bit line for input/output, D.
    • If we desire multiple bits, say *n* bits, for each address location, the entire structure must be duplicated *n* times.
  • The *enable line*, or often called chip select (CS), either allows the transmission gates to be closed or prevents them from being closed. This makes it so that the D can be in one of three modes;
    • reading, writing, or high impedance.
  • The ~*read/write* line controls which transmission gate is closed.
Memory Units
# Bits for Rows/Columns

- In general, given a certain size memory chip, such as a 1Mx1 memory chip, we would not know how the internal matrix is configured.
- For a 1Mx1 memory chip, we know it has 20 address lines (for our purposes in any case, there are exceptions in the real world). Any combination of address lines for the row and column decoder could be used to form the matrix.
  - Example: 10 row address lines and 10 column address lines for a 1024x1024 matrix of bit cells.
  - Example: 12 row address lines and 8 column address lines for a 4096x256 matrix of bit cells.
  - Example: 5 row address lines and 15 column address lines for a 32x32768 matrix of bit cells.
Memory Units
Multiple Bits (Words) I

- As noted, the described internal bit cell matrix structure accesses only 1 bit at a time.
- Multiple bits to form an $n$-bit word could be accessed in a few different methods.
  - One method is to have the column decoder select a set of $n$ columns simultaneously to form the word.
    - This only works if the entire word is stored in one row. Hence, there should be a multiple of $n$ columns in the bit cell matrix.
    - For instance, the given bit cell matrix with 8 columns could easily have words of size 1, 2, 4, or 8.
  - Another method, though arguably very similar, is to duplicate the entire bit cell matrix $n$ times to form the $n$-bit word.
Memory Units
Multiple Bits (Words) II

- The following illustrates these approaches for accessing a 4-bit word.

- On the left, **four column bits** from the **second row** are selected to form the **4-bit word**.
- On the right, the **first column bit** from the **second row** for **4 duplicates** of the bit cell matrix are accessed to form the **4-bit word**.
Building Systems
Designing Memory Systems

- What if we don’t have the right type of memory chips to build a desired computer system?
- Must learn to use combinations of existing memory chips to form a memory system according to specifications.
- Example: We want a **1Mx8** memory system but can only cheaply buy 1Mx4 memory chips. What to do?

Design a memory system that uses 1Mx4 memory chips but logically forms a 1Mx8 memory system.
Building Systems
Example #1

- Build a 1Mx8 memory system using 1Mx4 memory chips.
- First identify the specifications for the **1Mx4** memory chips and the desired **1Mx8** memory system?

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<td>1Mx4</td>
<td>4194304</td>
<td>1048576</td>
<td>20</td>
<td>4</td>
</tr>
</tbody>
</table>

- As the table shows, the # of addresses and # of address lines are the same for both. So, we do not have to change that.
- The number of data lines for the **1Mx8** are double that of the **1Mx4** as well as the total # of bits stored in the memory.
- Therefore, we require **two 1Mx4** memory chips arranged with the **same address lines** and **concatenated data lines**.
Building Systems
Example #1

- Forming the described 1Mx8 memory system with 1Mx4 chips, the following 1Mx8 memory system can be designed.
Building Systems
Example #2

- Build a 2Mx4 memory system using 1Mx4 memory chips.
  - First identify the specifications for the 1Mx4 memory chips and the desired 2Mx4 memory system?

<table>
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<td>4</td>
</tr>
</tbody>
</table>

- As the table shows, the # of data lines are the same for both.
- There is an extra address line in the 2Mx4 giving double the # of addresses and double the # of bits
  - Therefore, we require two 1Mx4 memory chips arranged where one address line is used to decode which 1Mx4 chip is enabled.
Building Systems
Example #2

- The following implements the desired 2Mx4 using 1Mx4 memory.

- Notice that $A_{20}$ is used to activate one of the 1Mx4 memory chips.
Memory Model
Programmer’s Model

- Goal is to abstract the memory model so that a programmer of the system does not need to know the physical layout of the memory.

- Below is an example $2^{32}$ addressable memory map of byte. This, for instance, could be implemented with a $4G\times 8$ memory system.

```
0x00000000  0x43
0x00000001  0x78
0x00000002  0x12
0x00000003  0x04
               ●
               ●
               ●
0xFFFFFFFF  0x7c
```
Memory Model

ENDIAN Byte Ordering (1)

• How should a multiple byte word be stored?
• The two most common orderings are
  • Big endian
    • The address is of the most significant byte location.
    • Sun Workstations and Macs use this ordering.
  • Little endian
    • The address is of the least significant byte location.
    • Intel x86 architectures use this ordering.

• Origins of the terms big and little endian.
  • Gulliver’s Travels: Feud between the two mythical islands, Lilliput and Blefescu, over the correct end (big or little) at which to crack an egg.
Memory Model
ENDIAN Byte Ordering (2)

- An example of a 4-byte word stored in big endian order
  - 0x12345678 would be stored as
    
    | 0x10010000 | 0x12 |
    | 0x10010001 | 0x34 |
    | 0x10010002 | 0x56 |
    | 0x10010003 | 0x78 |
    
    12345678

- An example of a 4-byte word stored in little endian order
  - 0x12345678 would be stored as
    
    | 0x10010000 | 0x78 |
    | 0x10010001 | 0x56 |
    | 0x10010002 | 0x34 |
    | 0x10010003 | 0x12 |
    
    78563412