Chapter 5
Internal Memory
Contents

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  — Organization
  — DRAM and SRAM
  — Types of ROM
  — Chip logic
  — Chip packaging
  — Module organization

• Error correction

• Advanced DRAM organization
  — Synchronous DRAM
  — Rambus DRAM
  — Cache DRAM
5.1 Semiconductor Main Memory

- Memory cell
  - Basic element of a semiconductor memory
  - Properties
    - exhibit two stable states for 1 and 0
    - can be written into
    - can be read from
Memory Cell Operation

(a) Write

(b) Read
# Semiconductor Memory Types

<table>
<thead>
<tr>
<th>Memory Type</th>
<th>Category</th>
<th>Erasure</th>
<th>Write Mechanism</th>
<th>Volatility</th>
</tr>
</thead>
<tbody>
<tr>
<td>Random-access memory (RAM)</td>
<td>Read-write memory</td>
<td>Electrically, byte-level</td>
<td>Electrically</td>
<td>Volatile</td>
</tr>
<tr>
<td>Read-only memory (ROM)</td>
<td>Read-only memory</td>
<td>Not possible</td>
<td>Masks</td>
<td></td>
</tr>
<tr>
<td>Programmable ROM (PROM)</td>
<td>Read-only memory</td>
<td></td>
<td></td>
<td>Nonvolatile</td>
</tr>
<tr>
<td>Erasable PROM (EPROM)</td>
<td>Read-mostly memory</td>
<td>UV light, chip-level</td>
<td>Electrically</td>
<td></td>
</tr>
<tr>
<td>Electrically Erasable PROM (EEPROM)</td>
<td>Read-mostly memory</td>
<td>Electrically, byte-level</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Flash memory</td>
<td></td>
<td>Electrically, block-level</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Semiconductor Memory

• RAM
  — Misnamed as all semiconductor memory is random access
  — Read/Write
  — Volatile
  — Temporary storage
  — Dynamic or Static
Dynamic RAM

- Bits are stored as charge in capacitors
  - Capacitors have tendency to discharge
  - Need refreshing even when powered
- Simpler construction (Fig 5.2(a))
  - Smaller circuit per bit
  - Less expensive
- Need refresh circuits
  - Slower
- Used for main memory
- Essentially analogue device
  - Level of charge determines value
Dynamic RAM (DRAM) Cell
DRAM Operation

• Address line active when bit read or written
  — Transistor switch closed (current flows)

• Write
  — Voltage to bit line
    - High for 1 and low for 0
  — Then signal address line
    - Transfers charge to capacitor

• Read
  — Address line selected
    - Transistor turns on
  — Charge from capacitor fed into the bit line
    - Compared with reference value to determine 0 or 1
  — Capacitor charge must be restored
Static RAM

• Bits are stored as on/off switches
  — No charges to leak
  — No refreshing needed when powered

• More complex construction
  — Larger circuit per bit
  — More expensive

• Does not need refresh circuits
  — Faster

• Used for cache

• Digital device
  — Uses flip-flops
Static RAM Operation

• Transistor arrangement gives stable logic state
  — State 1
    - $C_1$ high and $C_2$ low
    - $T_1$ $T_4$ off and $T_2$ $T_3$ on
  — State 0
    - $C_1$ low and $C_2$ high
    - $T_1$ $T_4$ on and $T_2$ $T_3$ off

• Transistors $T_5$ $T_6$ works as a switch
  — A signal applied, switch is on

• Write – apply value to B & compliment to $B$
• Read – value is on line B
Static RAM (SRAM) Cell
SRAM vs DRAM

- Both volatile
  - Power needed to preserve data
- Dynamic cell
  - Simpler to build, smaller
  - More dense
  - Less expensive
  - Needs refresh
  - Used for larger memory units
- Static cell
  - Faster
  - Cache
Read Only Memory (ROM)

- Permanent storage
  - Nonvolatile
- Applications
  - Microprogramming
  - Library subroutines
  - Systems programs (BIOS)
  - Function tables
Types of ROM

• Programmable ROM (once)
  — PROM
  — Needs special equipment to program

• Read “mostly” memory
  — Erasable Programmable (EPROM)
    - Before the write, all memory cells must be erased
    - Erased by UV light
  — Electrically Erasable (EEPROM)
    - Only the needed bytes can be updated
    - More expensive and less dense than EPROM
  — Flash memory
    - Possible to erase just blocks of memory (but not byte level)
    - Uses one transistor per bit (like EPROM)
**Chip Logic**

- **Organization of a 16 Mbit chip**
  - Can be organized as 1M of 16 bit words
  - Can be organized as one-bit-per-chip
  - Can be in between

- **A 16 Mbit chip as a 2048 x 2048 x 4 bit array**
  - Multiple DRAMs are connected to the controller to read/write a word
  - Reduced number of address pins
    - Multiplex row address and column address
    - 11 pins to each address \(2^{11}=2048\)
    - Adding one more pin doubles range of values so x4 capacity
 Refreshing

• Refresh circuit included on chip
• Refresh operation
  — Disable the chip
  — Count through all rows
    - For each row, data are read out and written back into the same location
• Takes time
• Slows down performance
Typical 16 Mb DRAM (4M x 4)
Memory Package Pins and Signals

(a) 8 Mbit EPROM

(b) 16 Mbit DRAM
A memory module of 256K 8-bit words
Module Organization (2)  A memory module of 1M 8-bit words
5.2 Error Correction

• Memory system is subject to errors
  – Hard failure
    - permanent physical defect
  – Soft failure
    - random, non-destructive event that alters the contents of memory cells

• Error-correcting/Error-detecting codes
  – Using some redundancy in data representation, we can correct/detect errors
Error Correcting Code Function

Text book, pages: 149 to 153
5.3 Advanced DRAM Organization

• Basic DRAM remains same since first RAM chips
• Enhanced DRAMs
  — SDRAM
  — RDRAM
  — CDRAM
Synchronous DRAM (SDRAM)

• Access in a typical DRAM
  — Address is presented to RAM
  — After access-time delay, DRAM reads/writes
  — Processor simply waits through this delay

• Access in SDRAM
  — Synchronized to an external clock
  — Address is presented to RAM
  — DRAM responds after a set number of clock cycles
  — CPU can do other tasks while SDRAM processing

• Employs a burst mode
  — A series of data bits can be clocked out rapidly after the first bit has been accessed

• DDR-SDRAM sends data twice per clock cycle
RAMBUS DRAM (RDRAM)

- Adopted by Intel for Pentium & Itanium
- Main competitor to SDRAM
- Vertical package – all pins on one side
  - Data exchange over 28 wires < 12 cm long
- RDRAM bus is used
  - Asynchronous block-oriented protocol
  - After 480ns initial access time, 1.6 GBps
  - Bus can address up to 320 RDRAM chips at 1.6 GBps
Cache DRAM (CDRAM)

• Developed by Mitsubishi
  — Integrates a small SRAM cache (16 Kb) onto a generic DRAM chip

• Cache usage
  — As a true cache
  — As a buffer to support the serial access of a block of data
    - (Ex) To refresh a bit-mapped screen, CDRAM can prefetch the data from DRAM into SRAM buffer